SESSION 5 – TAPA III
New FLASH and SRAM Developments

Thursday, June 17, 1:30 p.m.
Chairpersons: H. Pon, Intel
T. Kawahara, Hitachi

5.1 — 1:30 p.m.

A 0.13-µm, 0.78-µm^2 Low-Power Four-Transistor SRAM Cell with a Vertically Stacked Poly-Silicon MOS and a Dual-Word-Voltage Scheme, A. Kotabe, K. Osada, N. Kitai, M. Fujioka*, S. Kamohara*, M. Moniwa*, S. Morita* and Y. Saitoh*, Hitachi, Ltd., Tokyo, Japan, *Renesas Technology Corp., Tokyo, Japan

We developed a four-transistor SRAM cell with a vertically stacked poly-silicon MOS. Its size is 0.78 µm2 in a 0.13-µm technology, and only 38% of that of a six-transistor SRAM cell. By optimizing the device parameters of the cell transistors, and developing a modified electric-field-relaxation scheme, an estimated cell leakage current of 88.7 fA/cell was achieved. We also developed a dual-word-voltage scheme to achieve stable operation of the cell during a read operation.

5.2 — 1:55 p.m.

Modeling and Estimation of Failure Probability Due to Parameter Variations in Nano-Scale SRAMs for Yield Enhancement, S. Mukhopadhyay, H. Mahmoodi-Meimand and K. Roy, Purdue University, West Lafayette, IN

In this paper we have analyzed and modeled the failure probabilities (accesstime failure, read/write stability failure, and hold stability failure in the stand-by mode) of SRAM cells due to process parameter variations. A method to predict the yield of a memory chip designed with a cell is proposed based on the cell failure probability. The developed method can be used in the early stage of a design cycle to optimize the design for yield enhancement.

5.3 — 2:20 p.m.

A 0.9V 66MHz Access, 0.13µm 8M(256Kx32) Local SONOS Embedded Flash EEPROM, M.K. Seo, S.H. Sim, Y.H. Sim, M.H. Oh, S.W. Kim, I.W. Cho, H.S. Lee, G.H. Kim and M.G. Kim, Samsung Electronics Co., Ltd., Gyunggi-do, Korea

In 0.13µm CMOS logic compatible process, we implemented 256Kx32bit (8Mb) SONOS embedded flash EEPROM using ATD-assisted Current Sense Amplifier (AACSA) for 0.9V(0.7V~1.4V) low VCC application. Read operation is performed at a high frequency of 66MHz and shows a low current of typically 5mA at 66MHz operating frequency. Program operation is performed for common source array with wide I/Os(X32) by using Data-dependent Source Bias Control Scheme (DDSBCS). This novel SONOS embedded Flash EEPROM core has the cell size of 0.276um2 and the program and erase time of 20us and 20ms respectively

5.4 — 2:45 p.m.

Self-Boosted Charge Injection for 90-nm-Node 4-Gb Multilevel AG-AND Flash Memories Programmable at 16 MB/s, H. Kurata, K. Otsuga, Y. Sasago, T. Arigane, T. Kawamura, T. Kobayashi, Y. Ikeda*, A. Sato*, K. Kozakai*, S. Noda*, M.Shimizu*, O. Tsuchiya* and K. Furusawa*, Hitachi, Ltd., Tokyo, Japan, *Renesas Technology Corporation, Tokyo, Japan

This paper presents a high-speed multilevel programming scheme for 90-nm node AG-AND flash memories. Source-side hot-electron injection programming withself-boosted charge, accumulated in inversion-layer local bit-lines under AGs, reduces the dispersal of programming characteristics and also reduces the time overhead of pre-charging the bit-lines. With this self-boosted charge injection scheme, programming at a fast 16 MB/s is obtainable in 4-Gb flash memory with an actual cell size of 2F2/bit.

Break 3:10 p.m.